ABSTRACT OF THE DISCLOSURE

The present invention facilitates semiconductor device fabrication by providing mechanisms for utilizing different isolation schemes within embedded memory and other logic portions of a device. The isolation mechanism of the embedded memory portion is improved relative to other portions of the device by increasing dopant concentrations or reducing the depth of the dopant profiles within well regions of the embedded memory array. As a result, smaller isolation spacing can be employed thereby permitting a more compact array. The isolation mechanism of the logic portion is relatively less than that of the embedded memory portion, which permits greater operational speed for the logic.